Process Overview of Integration-Feasible Approaches for Achieving Area-Selective Deposition

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As the Si-based semiconductor industry goes into the sub-10 nm scale of its physical limit, conventional patterning processes, based on photolithography and etching, are facing fundamental limits for device downscaling. Accordingly, the deposition of atoms at specific locations on a desired surface can boost advances in catalysis, energy harvesting as well as semiconductor device fabrication. Of several paths being explored for novel bottom-up nanopatterning, area-selective atomic layer deposition (AS-ALD) is attracting increasing interest because of its ability to enable both continued dimensional scaling and accurate pattern placement for next-generation nanoelectronics. In this talk, we first explore general approaches and fundamental limitation of AS-ALD using self-assembled monolayers (SAMs). Accordingly, new opportunities can be opened up through development of alternative AS-ALD methods. In some efforts being pioneered, we introduce a topographical AS-ALD method using anisotropic ion implantation (with fluorocarbon implantation) and small alkylating agents such as aminosilanes. The efficacy of these alternative approaches shows promise for some of metal and oxide ALD systems. Lastly, we review some recent efforts for enabling selectivity improvement by implementing various process correction steps. In summary, we expect that continuous efforts advance practical applications that require area-selective coating of surfaces in a variety of nanostructures.